## REMARKS

Claims 10-17 are pending in the present application.

## Drawings

The Examiner has required that Figs. 9-12 be designated as "PRIOR ART". Accordingly, enclosed are (3) red-inked drawing Annotated Sheets, wherein Figs. 9-12 have been denoted as "PRIOR ART", as required. Also enclosed are three (3) drawing Replacement Sheets, incorporating the above noted corrections. **The Examiner is respectfully requested to acknowledge receipt and acceptance of the drawing Replacement Sheets.**

## Claim Rejections-35 U.S.C. 103

Claims 10-17 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Capote et al. reference (U.S. Patent No. 6,297,560) in view of the Riding et al. reference (U.S. Patent No. 6,083,811). This rejection is respectfully traversed for the following reasons.

The Examiner has primarily relied upon the Capote et al. reference as providing the semiconductor device including a semiconductor element, a sealing resin and a plurality of terminals, as featured in claim 10. The Examiner has noted that sealing resin 22 in Fig. 4 of the Capote et al. reference for example, has a thickness between about 15 μm and 200 μm, as described in column 6, lines 40-41. The Examiner has

however acknowledged that the Capote et al. reference "does not disclose a method wherein the semiconductor element 10 having a thickness of 200 microns or less and the sealing resin having a thickness equal to or greater than half a thickness of the semiconductor element".

In an effort to overcome these acknowledged deficiencies of the Capote et al. reference, the Examiner has relied upon the Riding et al. reference as including a semiconductor element 20 (Fig. 4) having a thickness of 4 mils (approximately 102 μm). The Examiner has alleged that it would have been obvious to use this semiconductor element thickness as taught by the Riding et al. reference with the method of the Capote et al. reference in the ranges claimed, "because it has been held that where the general conditions of the claims are disclosed in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation". Applicants respectfully disagree for the following reasons. In the Response to Arguments section beginning on page 5 of the Final Office Action, the Examiner has asserted that the criticality of the thickness stated has not been established.

As described on page 2 of the present application, problems of the conventional structure and manufacturing method include the occurrence of cracks at a junction between a semiconductor element and a mounting substrate due to thermal stress. Also, if the stress of a sealing resin is high, a warp develops in the resin sealing, which is difficult to fix when dividing the wafer into individual segments.

As described beginning on page 6, line 20 of the application, in order to solve

these problems, the semiconductor element is made thinner, so that the number of temperature cycles which the solder ball may endure before cracks appear increases. As further described beginning on page 7, line 6 of the present application, the flexibility of the semiconductor element itself increases with resultant better temperature characteristics, when the thickness of the resin is greater than the thickness of the semiconductor element.

Accordingly, cracks that occur primarily when mounting the semiconductor device on a substrate can be sufficiently restrained by setting the thickness of the semiconductor element to 200 μm or less, and by setting the thickness of the resin to one half or more of the thickness of the semiconductor element. Particularly, if this relative relationship between semiconductor element thickness and resin thickness is maintained, the occurrence of cracks may be restrained. The criticality of these thicknesses or values as expressed should be clearly understood in view of the above noted description and in view of Figs. 2A and 2B of the application.

The Capote et al. reference as relied upon by the Examiner discloses a thickness of encapsulate material or sealing resin in a range of 50 to 200 μm. However, as acknowledged by the Examiner, the Capote et al. reference does not disclose the thickness of chip 10. The Capote et al. reference thus does not disclose or suggest a relationship between semiconductor element thickness and sealing resin thickness, and more particularly does not disclose such a relationship that would reduce the occurrence of cracks at a junction between a semiconductor element and a

mounting substrate. Particularly, an objective of the Capote et al. reference is to eliminate the conventional capillary flow underflow process, not specifically to reduce the occurrence of cracks at a junction between a semiconductor element and a mounting substrate.

The Riding et al. reference as secondarily relied upon merely discloses that dice 20 has a thickness of 4 mils (about 100 μm). The Riding et al. reference does not specifically show a sealing resin. Accordingly, the Riding et al. reference does not disclose or suggest a relationship between semiconductor element thickness and sealing resin thickness, and more particularly does not disclose such a relationship that would reduce the occurrence of cracks at a junction between a semiconductor element and a mounting substrate. As such, the Riding et al. reference as secondarily relied upon by the Examiner does not overcome the acknowledged deficiencies of the primarily relied upon Capote et al. reference.

The Examiner has also apparently relied upon the newly presented Zenner et al. reference (U.S. Patent No. 6,246,010) in support of this rejection, even though this reference is not officially cited. However, the Zenner et al. reference also fails to disclose or suggest a relationship between semiconductor element thickness and sealing resin thickness, and does not disclose such a relationship that would reduce the occurrence of cracks at a junction therebetween.

Applicants therefore respectfully submit that the method of mounting a semiconductor device on a mounting substrate of claim 10 would not have been

obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 10-17 is improper for at least these reasons.

Claim 11 features that a thickness of a sealing resin on a peripheral portion of a semiconductor element that has a step part, is made to be greater than a thickness of the sealing resin on a central portion of the semiconductor element that is surrounded by the peripheral portion. The Examiner has relied upon Fig. 11 of the Capote et al. reference, apparently asserting that second portion 39 of the encapsulant material is a step part of the chip 10.

However, the Examiner has previously interpreted chip 10 of the Capote et al. reference as the semiconductor element of the claims. Chip 10 as shown in Figs. 3 and 4 of the Capote et al. reference does not include a peripheral portion having a step part. Accordingly, since chip 10 has no step part, the Capote et al. reference does not meet the features of providing a thickness of a sealing resin on a peripheral portion of a semiconductor element having a step part as being greater than a thickness of a sealing resin on a central portion of the semiconductor element. The Riding et al. reference as relied upon does not overcome these deficiencies. Applicants therefore respectfully submit that the method of claim 11 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claim 11 is improper for at least these additional reasons.

## Conclusion

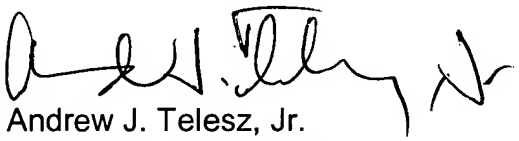
The Examiner is respectfully requested to reconsider and withdraw the corresponding rejection, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



Andrew J. Telesz, Jr.
Registration No. 33,581

One Freedom Square
11951 Freedom Drive, Suite 1260
Reston, Virginia 20190
Telephone No.: (571) 283-0270
Facsimile No.: (571) 283-0740

Enclosures: Three (3) red-inked Annotated Drawing Sheets
Three (3) Drawing Replacement Sheets

FIG.8

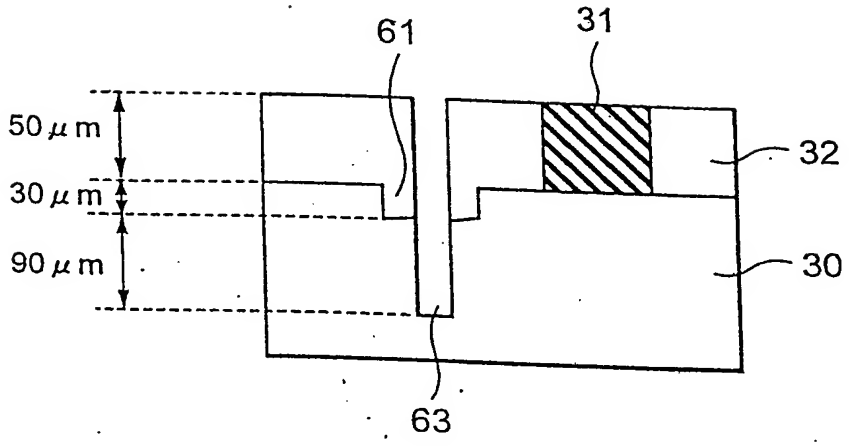
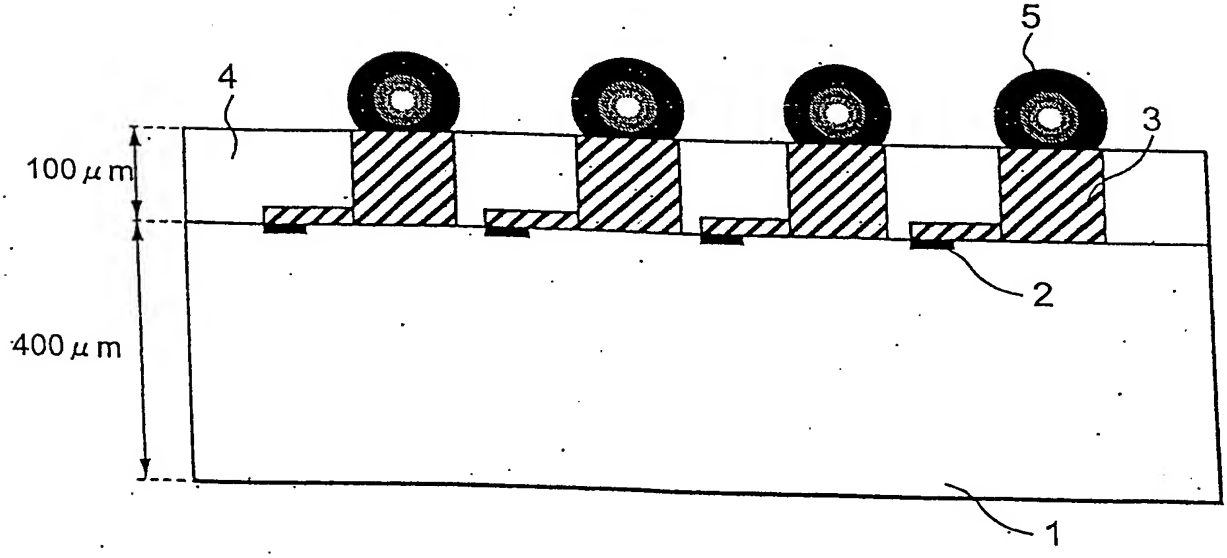



FIG.9
PRIOR ART



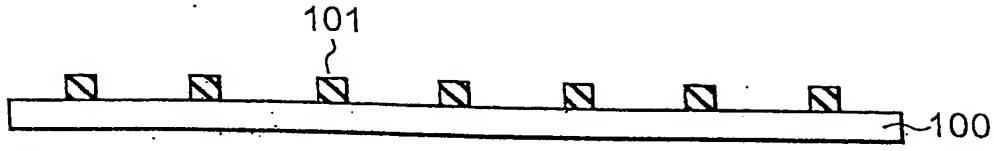



FIG.10A
PRIOR ART

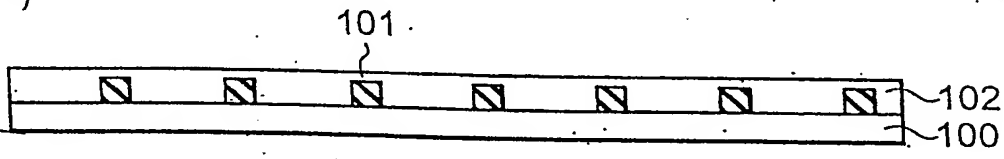



FIG.10B
PRIOR ART

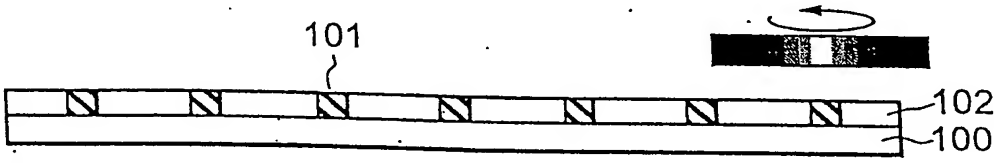



FIG.10C
PRIOR ART

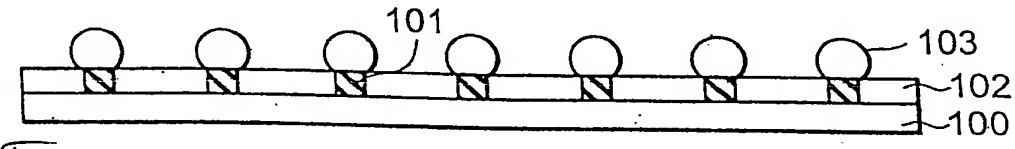



FIG.10D
PRIOR ART

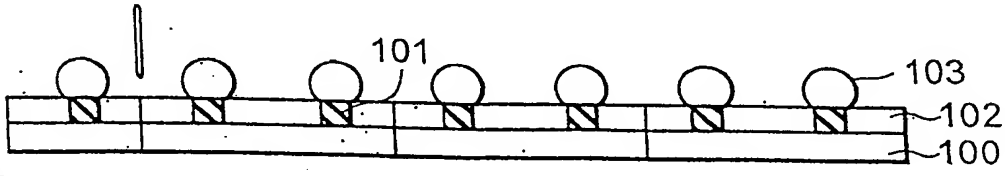



FIG.10E
PRIOR ART

FIG.11
PRIOR ART

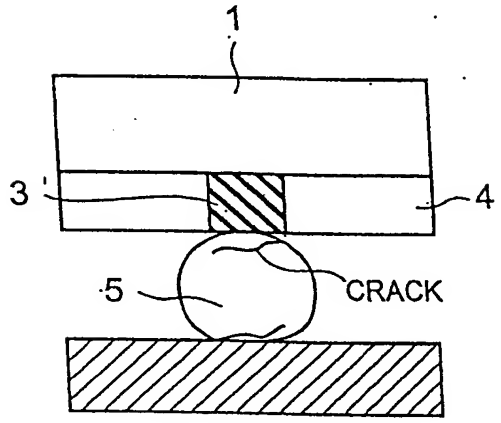



FIG.12
PRIOR ART